REMARKS

Applicants thank the Examiner for the Interview held on May 24, 2004 and for indicating that the amended claims appear to overcome the 35 U.S.C. §112 and the art rejections.

Claims 1-20 are pending. By this amendment, claim 20 is cancelled and claims 1, 8, and 15 are amended. No new matter is introduced. Support for the amendments may be found at least at page 4, lines 17-23, page 5, line 22 to page 6, line 7, page 6, line 26 to page 7, line 15, page 7, lines 2-15, and page 8, lines 8-24 of the specification and in original claims 2, 3, 4, 5, and 20. Reconsideration and allowance of the claims in view of the above amendments and the remarks that follow are respectfully requested.

Claim Rejections Under 35 U.S.C. §112

On page 2 the Office Action rejects claims 1-20 under 35 U.S.C. §112, ¶1, as failing to comply with the enablement requirement. This rejection is respectfully traversed.

The specification provides detailed and specific steps involved in the circuit simulation for determining the one margin and the zero margin in performing the DC analysis at least in Figures 1 and 3-6 and at page 6, line 13 to page 9, line 22 of the specification. For example, Figure 3 is a flow chart illustrating an exemplary method for performing the DC analysis of the simulated latch circuit and related elements, including steps 301, 302, 303, 304, and 305. On page 6, line 13 to page 9, line 22, the specification provides details with respect to each step involved in the DC analysis. Specifically, in step 301, a simulation is performed to determine the trip point voltage of the forward inverter of the latch (page 6, lines 14-16 and following text). In step 303, a simulation is performed to determine the one margin. An exemplary embodiment of the simulation circuit for the one margin determination is shown in Figure 5 (page 7, lines 21-22 and the following text). In step 305, a simulation is performed to determine the zero margin. An exemplary embodiment of the simulation circuit for the zero margin determination is shown in Figure 6 (page 9, lines 2-3 and the following text). Moreover, specific program listing are provided in Appendix on pages 11-19. One skilled in the art to which it pertains will be able to make and use the claimed invention without resorting to undue experimentation.

On page 3 the Office Action rejects claims 1-20 under 35 U.S.C. §112, ¶1, as failing to comply with the written description requirement. This rejection is respectfully traversed.

As stated above with respect to the enablement requirement, the specification provides detailed and specific steps involved in the circuit simulation for determining the one margin and the zero margin in performing the DC analysis at least in Figures 1 and 3-6 and at

page 6, line 13 to page 9, line 22 of the specification. One skilled in the relevant art will recognize that the inventors, at the time the application was file, had possession of the claimed invention. Withdrawal of the claim rejections under 35 U.S.C. §112 is respectfully requested.

Claim Rejections Under 35 U.S.C. §102

On page 4 the Office Action rejects claims 1, 8, and 15 under 35 U.S.C. § 102(b) over U.S. Patent 6,292,766 to Mattos et al. (hereafter Mattos). This rejection is respectfully traversed.

Mattos is directed to a simulation tool input file generator for interface circuitry. However, Mattos does not disclose or suggest "determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element," as recited in amended claim 1. As acknowledged by the Examiner during the Interview, Mattos does not disclose or suggest the step of determining a worst case pull-up path and a worst case pull-down path. Accordingly, Mattos does not disclose or suggest all the features of claim 1, and claim 1 is patentable.

Claim 8 is a computer readable storage medium claim generally corresponding to patentable method claim 1. In particular, claim 8, as amended, recites "determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element." As discussed above with respect to claim 1, the feature of determining a worst case pull-up path and a worst case pull-down path is not disclosed or suggested by Mattos. Accordingly, claim 8 is patentable.

Claim 15 is an apparatus claim generally corresponding to patentable method claim 1. In particular, claim 15, as amended, recites "wherein the worst case signal path is determined analytically by accumulating a weighted resistance of each circuit element along the plurality

of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element." As discussed above with respect to claim 1, the feature of determining a worst case path is not disclosed or suggested by Mattos. Accordingly, claim 15 is patentable.

On page 5 the Office Action rejects claims 1, 8, and 15 under 35 U.S.C. § 102(b) over "MicroSim PSpice A/D Reference Manual" (hereafter MicroSim). This rejection is respectfully traversed.

MicroSim is a manual containing reference material needed when working special circuit analysis in PSpice A/D. However, MicroSim does not disclose or suggest "determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element," as recited in amended claim 1. MicroSim uses brute force approach to simulate all paths and does not determine which path to simulate selectively. Therefore, amended claim 1 is patentable over MicroSim.

Similarly, MicroSim does not disclose or suggest "determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element," as recited in amended claim 8. Therefore, amended claim 8 is patentable over MicroSim.

Likewise, MicroSim does not disclose or suggest "wherein the worst case signal path is determined analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the

signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element," as recited in amended claim 15. Therefore, amended claim 15 is patentable over MicroSim. Withdrawal of the rejection of claims 1, 8, and 15 under 35 U.S.C. § 102(b) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

On page 6 the Office Action rejects claims 2-7, 9-14, and 16-20 under 35 U.S.C. § 103(a) over MicroSim in view of "Fast generation of statistically-based worst-case modeling of on-chip interconnect, N. Chang et al." (hereafter Chang). This rejection is respectfully traversed.

Claim 20 is cancelled, rendering the rejection of claim 20 moot.

To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) must teach or suggest all of the claim limitations. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and MPEP § 2142. If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and MPEP § 2143.03.

Chang discloses finding the worst case of a circuit with a statistical equation and using weighting to match real world performance. However, Chang does not disclose or suggest using a weight to increase the resistance of a circuit element depending on the signal passing through the circuit element and the voltage drop. In addition, Chang does not disclose or suggest determining a worst case pull-up/pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths.

Therefore, MicroSim and Chang, individually and in combination, do not disclose or suggest "determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element," as recited in amended claim 1. Therefore, amended claim 1 is patentable over MicroSim and Chang.

Similarly, MicroSim and Chang, individually and in combination, do not disclose or suggest "determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a

topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element," as recited in amended claim 8. Therefore, amended claim 8 is patentable over MicroSim and Chang.

Likewise, MicroSim and Chang, individually and in combination, do not disclose or suggest "wherein the worst case signal path is determined analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element," as recited in amended claim 15. Therefore, amended claim 15 is patentable over MicroSim and Chang.

Claims 2-7, 9-14, and 16-19 depend on the respective independent claims 1, 8, and 15, which, as noted above, are patentable. For this reason and the additional features they recite, claims 2-7, 9-14, and 16-19 are also patentable. Withdrawal of the rejection of claims 2-7, 9-14, and 16-20 is respectfully requested.

In view of the above remarks, Applicants respectfully submit that the application is in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

Date: **May 27, 2004**

Kelly T. Lee
Registration No. 47,743
Andrews Kurth LLP
1701 Pennsylvania Ave, N.W.
Suite 300
Washington, DC 20006
Tel. (202) 662-2736
Fax (202) 662-2739